Design Considerations for Ultra-Low Energy Wireless Micro Sensor Nodes

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ABSTRACT

This tutorial paper examines architectural and circuit design techniques for a micro sensor node operating at power levels low enough to enable the use of an energy harvesting source. These requirements place demands on all levels of the design. We propose architecture for achieving the required ultra-low energy operation and discuss the circuit techniques necessary to implement the system. Dedicated hardware implementations improve the efficiency for specific functionality, and modular partitioning permits fine-grained optimization and power-gating. We describe modeling and operating at the minimum energy point in the transmitter and the ADC. A micro sensor node using the techniques we describe can function in an energy-harvesting scenario

Kewords: Integrated circuits, energy-aware systems, low-power design, wireless sensor networks

1. INTRODUCTION

WIRELESS microsensor networks consist of ten to thousands of distributed nodes that sense and process data and relay it to the end-user. Applications for wireless sensor networks range from military target tracking to industrial monitoring and home environmental control. The distributed nature of micro sensor networks places an energy constraint on the sensor nodes. Typically, this Constraint is imposed by the capacity of the node's battery For this reason, most micro sensor networks duty cycle, or shutdown unused components whenever possible. In this paper, duty cycling refers generically to alternating between an active mode and a low-power sleep mode. Although duty cycling helps to extend sensor network lifetimes, it does not remove the energy constraint placed by the battery. For some applications, a limited lifetime is sufficient and battery power is the logical choice. A 1cm Lithium battery can continuously supply 10 W of power for five years. This tutorial focuses on applications demanding higher peak power or longer lifetime in an environment where changing batteries is impractical or impossible, therefore requiring a renewable energy source

Research into energy scavenging suggests that micro sensors can utilize energy harvested from the environment Energy harvesting schemes convert ambient energy into electrical energy, which is stored and utilized by the node the most familiar sources of ambient energy include solar power, thermal gradients, radio-frequency (RF), and mechanical vibration. Table 1 gives a comparison of some energy harvesting technologies. Power per area is reported because the thickness of these devices is typically dominated by the other two dimensions. The power available from these sources is highly dependent on the nodes environment at any given time. However, these examples show that it is reasonable to expect 10s of microwatts of power to be harvested from ambient energy. Barring significant advances in energy scavenging technology, the high instantaneous power consumption of an active wireless transceiver (mill watts for Mbps) requires micro sensors to retain local energy storage. Coupling energy harvesting techniques with some form of energy storage can theoretically extend micro sensor node lifetimes indefinitely.

Using a rechargeable energy reserve with energy-harvest in implies several constraints for improving node efficiency First, the standby power of the node must be less than the average power supplied by the

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energy-harvesting mechanism. If this is not the case, then energy-harvesting cannot recharge the battery and the nodes will expire. Second, the node should use as little energy as possible during active operation. Minimizing energy per operation allows decreased energy storage capacity (size, weight, and cost) and/ or a higher duty cycle (better performance). Third, the node should make gracefull transition to and from standby mode with very little time or energy overhead, increasing the efficiency of duty cycling for extremely short periods of time in the active mode.

2. MICRO SENSOR NODE ARCHITECTURE

The AMPS-1 sensor node, a representative node example, provides a hardware platform for distributed micro sensor networks using commercial, off the-shelf (COTS) components.
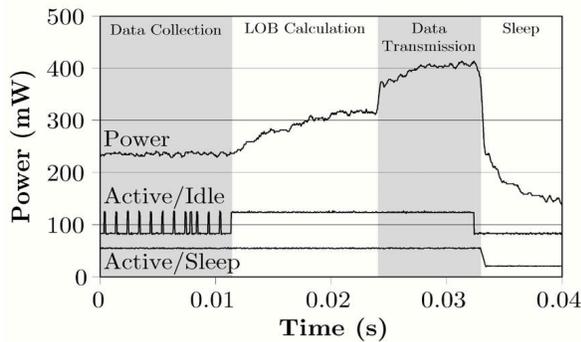
Fig. 1: Power-scaling measurements on the AMPS-1 node

The sensor node processor uses dynamic voltage scaling (DVS) to minimize energy consumption for a given performance requirement. The radio transmit power adjusts to one of six levels, depending on the physical location of the target nodes. Power consumption of the node varies from 3.5mW in the deepest sleep state up to almost 2W (1.1W of which goes into the transmitter power amplifier) with the processor running at the fastest clock rate and the radio transmitting at the highest power level. Fig. 1 shows the instantaneous power consumption of a AMPS-1 node as it collects data samples from the microphone, performs a line-of-bearing (LOB) calculation on the collected data, and relays the results of this calculation to other nearby nodes. Using generic components makes the power too high for the

constraints we have described, so a customized architecture is necessary.

The energy savings of a custom approach come from modularizing the sensor node by considering common tasks for sensor network applications. Key tasks which can be implemented in hardware include the fast Fourier transform (FFT), finite impulse response (FIR) filters encryption, source coding, channel coding/decoding, and Encryption, source coding, channel coding/decoding, and interfaces for the radio and sensor. In order to achieve energy efficiency throughout the entire system, the hardware modules can use independent voltage supplies and operate at different clock frequencies. The drawbacks of this architecture are the increase in system complexity and area the need for additional data transfers between the DSP and specialized modules, and the difficulty of interoperability across different voltage and clock islands.

Fig.2 shows our proposed architecture for an energy efficient sensor node. The digital architecture contains a simple DSP that executes arbitrary programs. The DSP communicates with the specialized modules through a shared bus and the DMA schedules the transfer of data between modules and the bus. Data memory is accessible by both the specialized modules and the DSP.
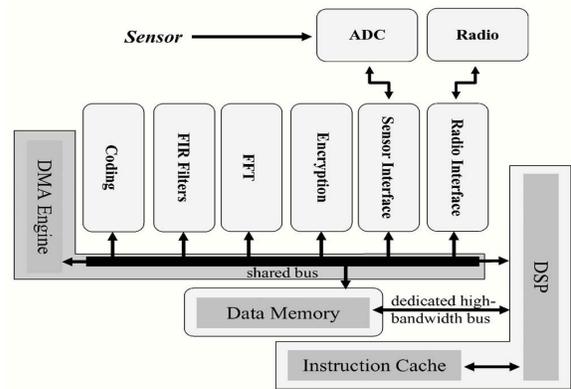
Fig. 2: Proposed architecture of an energy-efficient sensor node

Dynamic voltage scaling (DVS) can be used to trade energy for computational latency for each module. A module's supply voltage should be set to the lowest possible value that satisfies its speed requirements. However, there is a supply voltage

below which computations become less energy efficient due to leakage currents .When no computation is taking place, the supply voltage should be shut off from the CMOS logic to reduce leakage power. The analog modules require the same dynamic performance controls as the digital modules. Both the sensor and radio must have an "always on," low-power standby mode that allows for basic threshold detection of a wake-up signal. For instance, an audio sensor might operate in a low-power mode until sound of a certain magnitude is detected.

3. DIGITAL CIRCUIT TECHNIQUES

Digital circuit design for the micro sensor space must focus primarily on the energy and power constraints we have presented, rather than solely on maximizing performance .The unpredictable environment of micro sensor networks coupled with less stringent performance requirements allows a trade-off of speed for reduced energy at both the architecture and circuit levels.

3.1 Sub threshold Operation

When minimizing energy is the primary system requirement, the sub threshold region gives the minimum energy solution for most circuits. Sub threshold circuits use a supply voltage V_{DD} that is less than the threshold voltage, V_T voltage of the transistors. In this regime, sub threshold leakage currents charge and discharge load capacitances
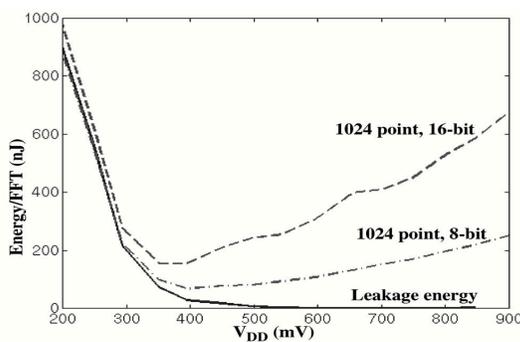
Fig 3: Energy of FFT processor vs. Energy Leakage

Limiting performance but giving significant energy savings over nominal V_{DD} operation. Fig. 3 gives an example of sub threshold operation for a 0.18 m CMOS technology. The left-hand plot shows the measured frequency of a ring oscillator versus V_{DD}, Once V_{DD} drops into the subthres-hold region, the on-current of the transistors becomes exponential with voltage and the

$I_{on} = I_{off}$ ratio reduces quickly. This causes the delay to increase exponentially. The right-hand plot shows an oscilloscope plot of an FIR filter operating at 150mV and 3.2 kHz.

Fig. 3 shows give measurements from a sub threshold FFT processor that shows how minimum energy operation does not necessarily occur at minimum voltage operation. The 0.18 m CMOS chip implements a 1,024-point, 16-bit FFT A new sub threshold design methodology using a modified standard logic cell library, custom multiplier and memory generators was employed to implement the processor without additional process steps or body-biasing The processor operates down to 180mV, where it runs at 164Hz and 90nW. The figure shows the minimum energy point for the 16b, 1,024-pt FFT processor at 350mV, where it dissipates 155nJ/FFT at a clock frequency of 10 kHz. As V_{DD} decreases, the switching energy reduces quadratically. But propagation delay increases exponentially in the sub threshold region, allowing leakage current to integrate longer for each operation. The resulting increase in leakage energy causes the minimum energy point. For 8-bit operation, the minimum energy point moves to higher V_{DD} Since the scenarios, we present a model for finding minimum energy operation in the sub threshold region.

3.2 Sub threshold Energy Modeling

In order to develop a model for sub threshold operation of arbitrary circuits, we first examine the sub threshold propagation delay of a characteristic inverter.

3.3 Standby Power Reduction
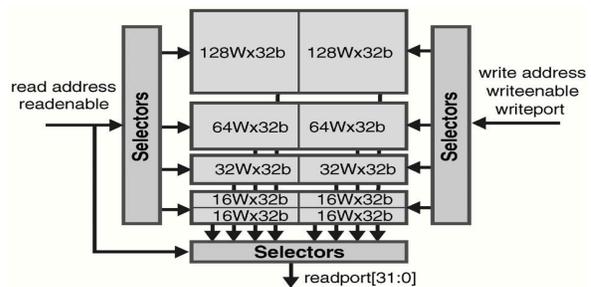
Fig 4: Scalable FFT memory that enables variable memory size

In the energy-aware FFT architecture in fig. 4 described earlier signals are gated to improve energy efficiency. This technique reduces active power dissipation, but leakage power is not affected. As nanometer CMOS processes are leveraged to improve performance and energy-efficiency leakage mitigation becomes an increasingly important design consideration. Deep submicron processes have increased sub threshold leakage, gate leakage, gate-induced drain leakage, and reverse biased diode leakage [13].
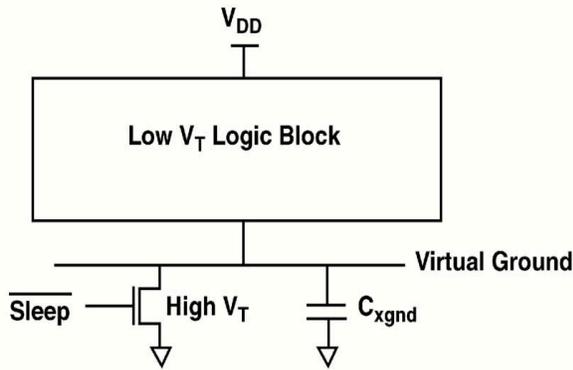
Fig.5: MTCMOS power-gating circuits for standby power reduction

The literature contains many techniques for standby power reduction. Two promising approaches for micro sensor nodes are multi-threshold CMOS (MTCMOS) and standby Voltage scaling Fig. 5 shows how MTCMOS circuits reduce standby leakage power by severing a circuit from the power rails with high VT sleep devices . Sizing the sleep transistor has received a lot of attention since over sizing limits the leakage savings while under sizing restricts performance Likewise, designing sequential MTCMOS circuits takes special care to reduce leakage during sleep without losing state Most MTCMOS designs use large sleep devices at the block level, but local sleep devices allow circuit partitioning into local sleep regions. Any unused circuit regions can enter sleep mode while surrounding circuits remain active. This approach only provides savings if all leakage currents are prevented during sleep mode. A careful design methodology can prevent subtle leakage paths from occurring at the MTCMOS interface to active circuits. A fabricated 0.13- m, dual

V T CMOS test chip shows low power FPGA architecture with over 8X measured standby current reduction [19]. The local sleep regions reduce active chip leakage by up to 2.2X for some configurations. The test chip uses sequential elements that allow power gating without the loss of data.

3.4 ADC and Sensor Subsystem

In sensor nodes, where a low-power DSP performs application-level processing, a front-end analog-to-digital conversion system acquires data from the physical sensor Since the ADC requirements are tightly coupled to a generally unpredictable environment, the ability to dyna- mically compromise features and performance in favor of power reduction is a valuable characteristic. In the limit, the ADC subsystem may act only as a threshold detector. This requires downstream data processing units to tolerate the compromises and to provide feedback to the ADC

Subsystem regarding the desired operating mode. Factors affecting that decision feedback might include characteristics of the sensing environment or the availability of harvested energy. This section examines a number of dimensions along which scaling could have a significant effect on overall power for the sensor front-end and ADC .The design of a low power ADC subsystem requires consideration of the entire front-end, not just the ADC.
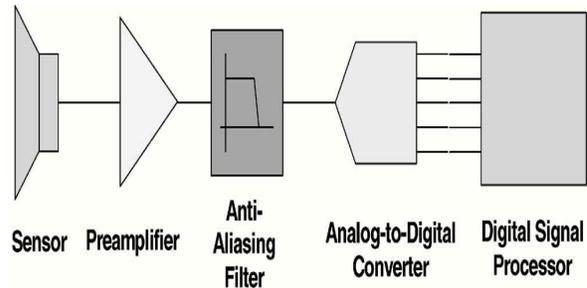
Fig. 6 : ADC subsystem

Fig. 6 shows a very simple ADC subsystem. The components shown include a sensor, a low-noise preamplifier, an ant aliasing filter, an ADC, and a DSP. Here, the DSP may be used for the application of ADC linearity calibration coefficients offset/gain error cancellation or digital decimation filtering.

In the case of low-event sensor nodes, optimizations in three critical states have been

identified. These include

1. As used here, the power consumption of the physical sensor would be prohibitive to a self-powered node. Innovations in sensor technology or customized raw transducers are required.

2. This factor does not consider an increase in unit capacitances required in order to improve matching characteristics of fabricated elements

3. Some minimal circuitry to manage standby-to-active state transitions such as a counter, might impose additional overhead

4. CONCLUSION

This paper describes the challenges facing wireless micro- sensor design and presents general micro sensor node architecture. The challenge for next generation nodes is to further reduce energy consumption by optimizing energy awareness over all levels of design. Sub threshold operation power gating, and standby voltage scaling enable digital circuits to meet the low active energy and standby power requirements of micro sensor nodes. Reducing startup time improves the energy efficiency of a transmitter for short packets and multi routing reduces energy for long- distance communication. Since the ADC subsystem might be the front-end of a reactive sensor node, it is important to seek alternatives to full sleep modes. We analyzed the dimensions along which ADC performance might be compromised in order to recover power savings. Applying all of these techniques to a micro sensor node makes energy-harvesting operation a possibility for micro sensor networks.

REFERENCES

[1]   S. Roundy, P. Wright, and J. Rabaey, "A Study of Low Level Vibrations as a Power Source for Wireless Sensor Nodes," Computer Comm., vol. 26, no. 11, pp. 1131-1144, July 2003

[2]   H. Kulah and K. Najafi, "An Electromagnetic Micro Power Generator For Low-Frequency Environmental Vibrations," Proc 17th IEEE Int'l Conf. Micro Electro Mechanical Systems (MEMS) pp. 237-240, Jan. 2004

[3]   S. Meninger et al., "Vibration-to-Electric Energy Conversion," IEEE Trans. Very Large Scale Integration (VLSI) Systems, vol. 9, no. 1 pp. 64-76, Feb. 2001

[4]   H. Bottner et al., "New Thermoelectric Components Using Microsystem Technologies," J. Micro Electro Mechanical Systems vol. 13, no. 3, pp. 414-420, June 2004

[5]   "Panasonic Solar Cell Technical Handbook '98/99," Aug. 1998

[6]   J.M. Kahn, R.H. Katz, and K.S. J. Pister, "Next Century Challenges: Mobile Networking for 'Smart Dust'," Proc. Mobicom 1999, pp. 271278, 1999

[7]   J. Rabaey et al., "PicoRadio Supports Ad Hoc Ultra-Low Power Wireless Networking," Computer, pp. 42-48, July 2000.

[8]   A. Wang and A.P. Chandrakasan, "A 180 mV FFT Processor Using Subthreshold Circuit Techniques," Proc. Int'l Solid-States Circuits Conf. (ISSCC), pp. 292-293, Feb. 2004.

[9]   A. Wang, A. Chandrakasan, and S. Kosonocky, "Optimal Supply and Threshold Scaling for Subthreshold CMOS Circuits," Proc Symp. VLSI, pp. 5-9, 2002

[10]   J. Burr and A. Peterson, "Ultra Low Power CMOS Technology," Proc. Third NASA Symp. VLSI Design, pp. 4.2.1-4.2.13, 1991

[11]   B.H. Calhoun and A. Chandrakasan, "Characterizing and Modeling Minimum Energy Operation for Subthreshold Circuits," Proc Int'l Symp. Low Power Electronics and Design (ISLPED), Aug. 2004

[12]   K. Osada et al., "SRAM Immunity to Cosmic-Ray-Induced Multierrors Based on Analysis of an Induced Parasitic Bipolar Effect," IEEE J. Solid State Circuits, vol. 39, no. 5, pp. 827-833, May 2004

[13]   R.H. Walden, "Analog-to-Digital Converter Survey and Analysis IEEE J. Selected Areas in Comm., vol. 17, no. 4, pp. 539-550, Apr 1999

[14]   M. Bhardwaj, T. Garnett, and A. Chandrakasan, "Upper Bounds on the Lifetime of Sensor Networks," Proc. IEEE Int'l Conf. Comm., pp. 785-790, 2001

[15]   J. Kao and A. Chandrakasan, "MTCMOS Sequential Circuits Proc. European Solid State Circuit Conf. (ESSCIRC), 2001

[16]   F.M. Gardner, Phase Lock Techniques. New York: Wiley, 1979

[17]   S.H. Cho and A.P. Chandrakasan,"6.5GHz CMOS FSK Modulator for Wireless Sensor Applications," IEEE Symp. VLSI Circuits, pp. 182-185, 2002.